A Low Cost Single Chip VDL Compatible Transceiver ASIC

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Introduction

- **Rationale for a Single Chip Radio**
- **Chip Architecture**
- **Radio Chip Specification**
- **Application Demonstration System**
- **Conclusion**

Rationale for Radio on a Chip

- Commercial communications system components increasingly focussed on cellular telephone technology.
  - Larger market than general purpose radio circuits
  - Many traditional sources of generic radio components have quit the market.
  - General purpose radio chip market is too small & profits too limited to appeal to most chip vendors

Rationale for Radio on a Chip

- Bring technology into the Aeronautical sector
  - Reduces issues with obsolescence
    - reduces product life cycle costs
- Custom designs tailored to specific applications
  - Designed specifically for avionics market
- Reduced component counts are possible
  - Highly integrated designs mean fewer external components

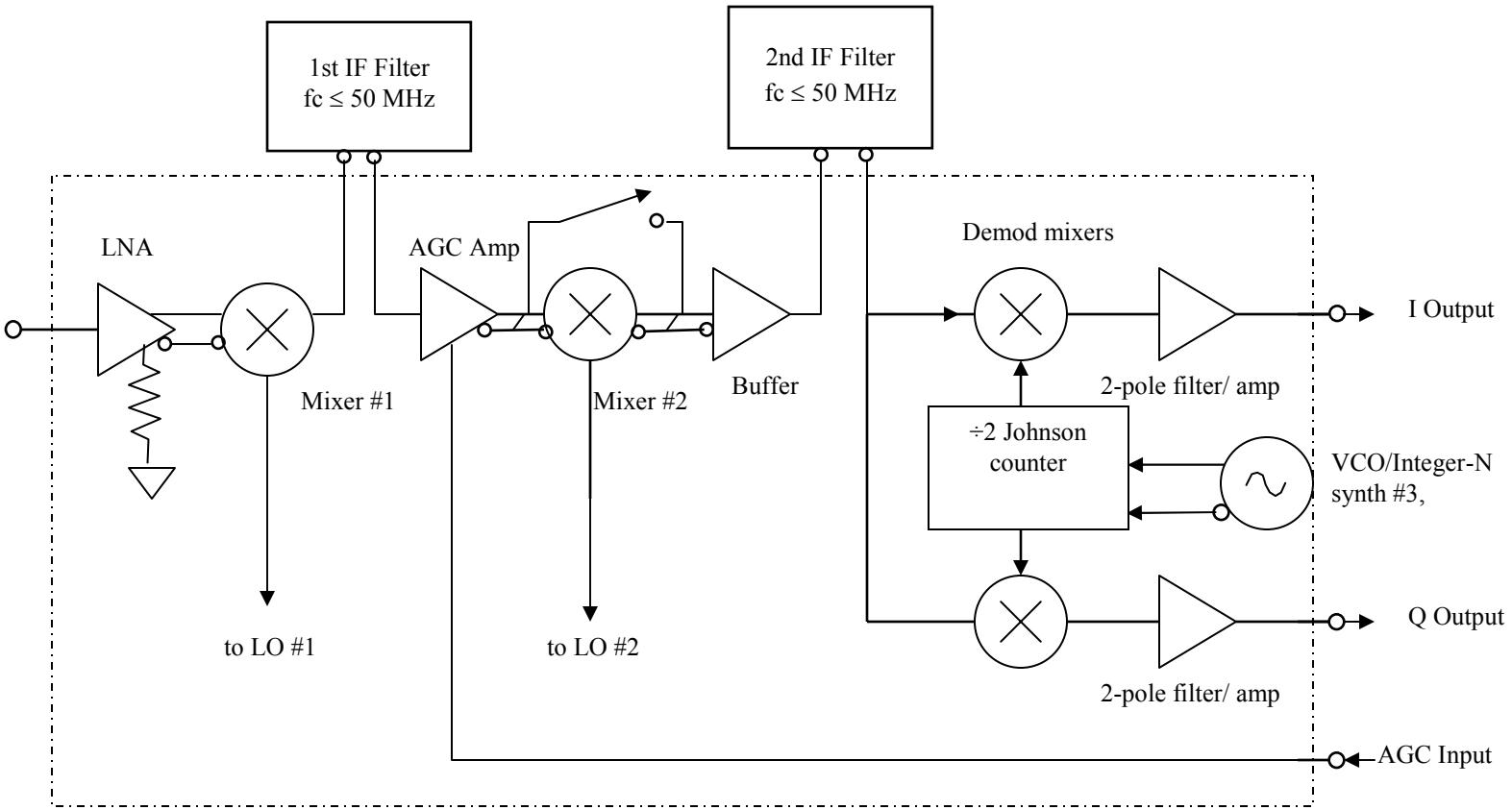
Rationale for Radio on a Chip

- Control obsolescence
  - Dependence on vendor removed
- Control performance parameters
  - Able to tailor performance to your requirements

Rationale for Radio on a Chip

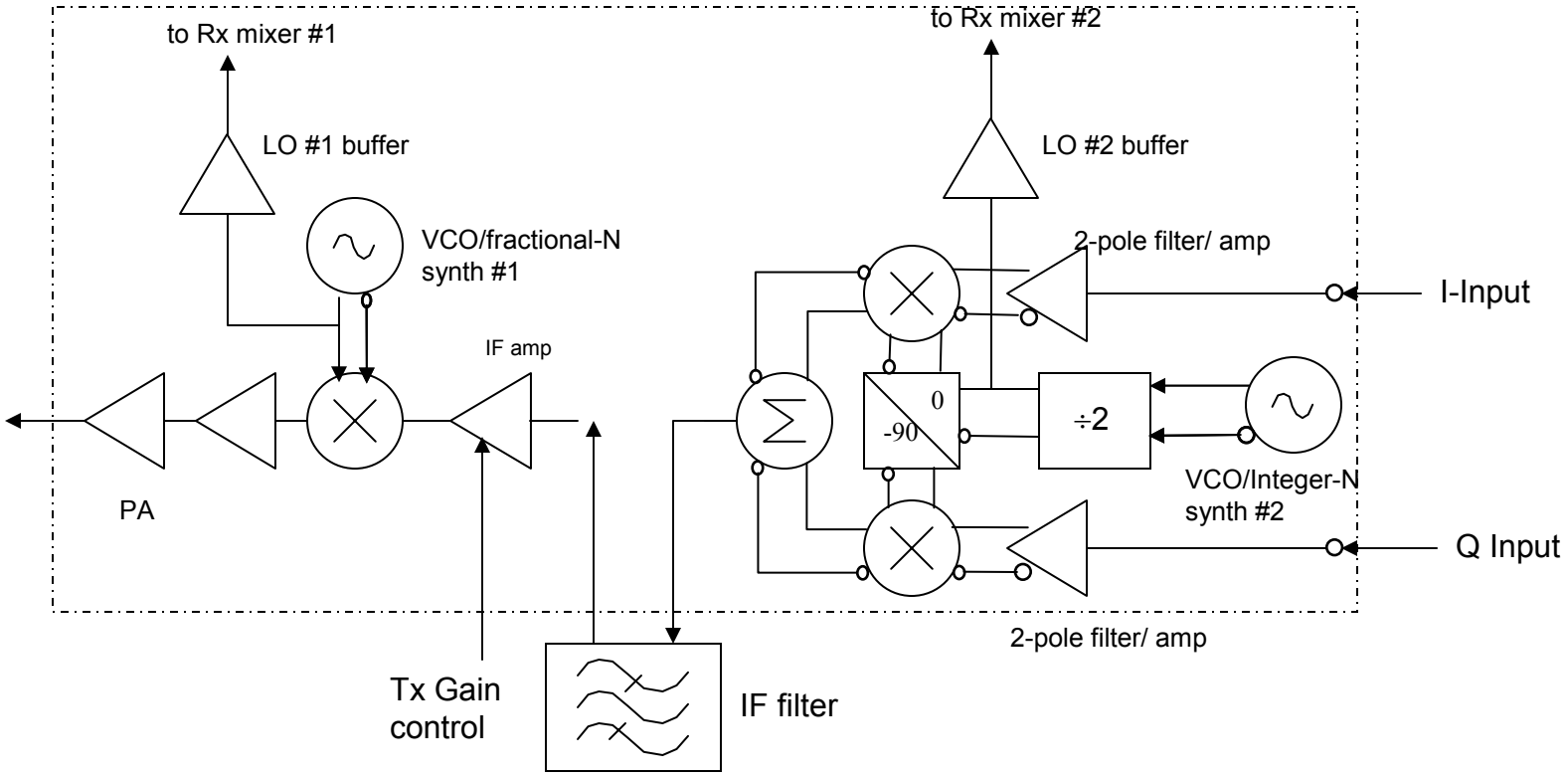
- Expensive to create
  - Design costs typically exceed $1M
- Limited markets
  - Some compromises may be required to increase the market for the design (cost spreading)
  - Per unit costs may run higher than commercial components
- Dependence on foundry process cycles
  - Process for making the chip can go obsolete

Chip Architecture - Rcvr



Receiver

Chip Architecture - Xmtr



Transmitter

Chip Architecture, cont'd

- Super-heterodyne single/double (switchable) conversion receiver
  - Can be used in either single or double conversion mode
  - Higher performance than direct conversion receivers
  - Better noise figure than direct conversion receivers
  - Higher IP3 point than direct conversion systems

Chip Architecture, cont'd

- Why not a more software defined design?
  - Software defined radios are extremely flexible
  - Can adapt to new modulation types with firmware modifications
  - Significant designer control over performance
  - Software radios cost point is higher
  - Maturity of the technology
  - Too power hungry for battery powered applications
    - ill suited to low power applications.

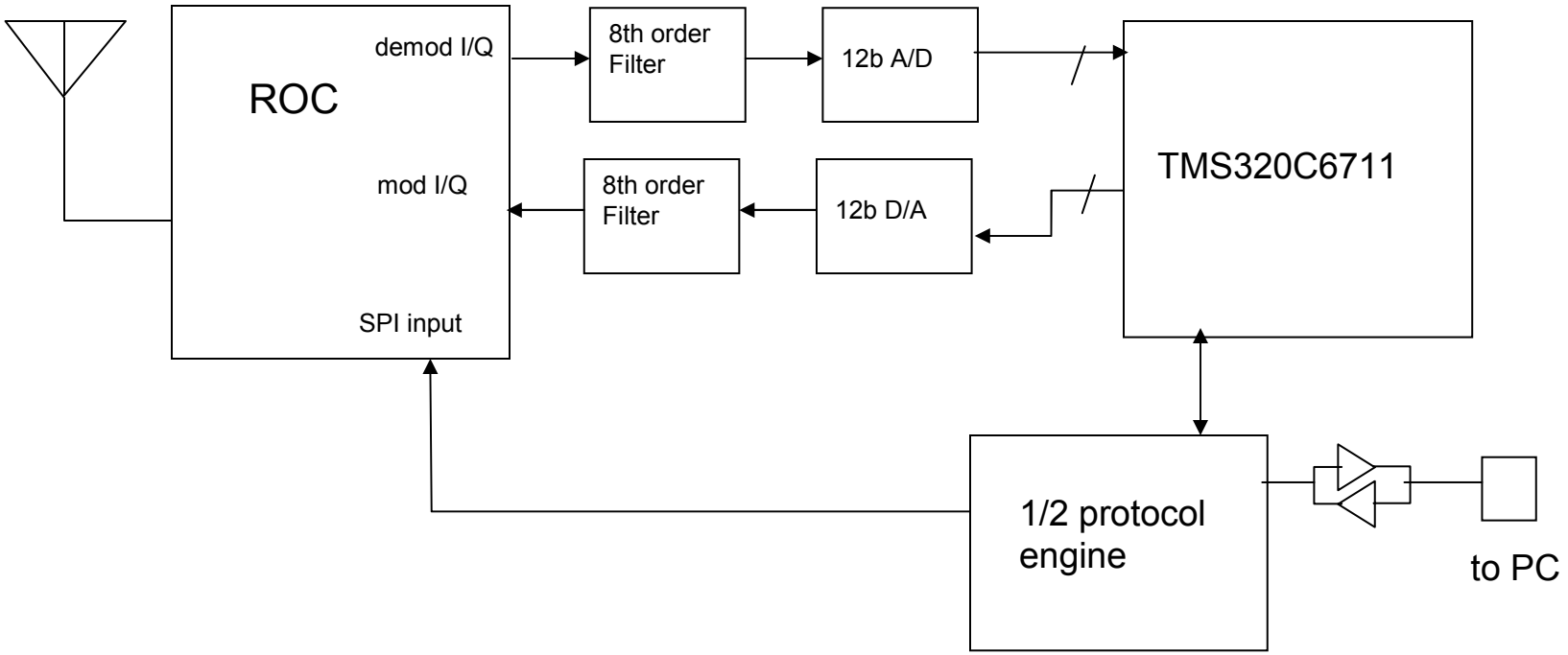
Chip Architecture, cont'd

- Analog I/Q demodulator
  - Lower overall power consumption than digital down-conversion and demodulation
  - Uses Johnson counters for nearly perfect I/Q LO generation
- Three integrated local oscillators
  - external tank and tuning components required.

Chip Architecture, cont'd

- Fully integrated synthesizers for all LO's
  - Integer-N designs for the 2nd & 3rd LO
  - Fractional-N for the 1st LO
    - Offers improved LO noise vis-à-vis integer-N designs
    - Faster frequency switching than integer-N synthesizers.

System Architecture



Transceiver architecture is very simple

Application Range

- Initial target is low cost devices
  - cost sensitive market
  - widest possible ranges of users
    - EFB - Air Transport
    - Low cost NEXCOM transceiver - General Aviation
  - graduate to expanded markets with later designs
- Battery operation
  - independent of aircraft systems

Application Range

- Target operating range is 50MHz to 450MHz
  - Covers marker beacon, comm, nav, ILS, glideslope, & MilCom bands
    - larger application market means lower per-unit costs

Application Range

- Present design targets for VDL applications
  - Present IIP3 point is too low for fully certified NEXCOM communications products
  - Future designs will address higher degrees of certification

Chip Specifications

DC Characteristics (25 °C)

Parameter	Conditions	Min.	Typ.	Max.	Units
Power supply	Vdd Idss	3.0 40		5.0 75	V mA
Logic Interface	Vih (3.0V < Vdd < 5.0V) Vil (3.0V < Vdd < 5.0V) Voh (3.0V < Vdd < 5.0V, Isrc < 3 mA) Vol (3.0V < Vdd < 5.0V, Isink < 10 mA)	Vdd/2 + 0.6 Vss Vdd – 0.5 0.4		Vdd + 0.6 0.8 Vdd – 0.5 0.5	V V V V

Chip Specifications

AC Characteristics

Parameter	Conditions	Min.	Typical	Max	Units
Operating frequency range		20		450	MHz
Rx noise figure			4		dB
Rx IIP3			4		dBm
1st IF bandwidth	-3dB bandwidth	2		45	MHz
2nd IF bandwidth	-3dB bandwidth			15	MHz
I/Q demodulator bandwidth	-3dB bandwidth			1	MHz
Demodulator output				1	Vp-p
I/Q modulator bandwidth	-3dB bandwidth			1	MHz
I/Q modulator input				1	Vp-p
I/Q Modulator bandwidth	-3dB bandwidth	5		70	MHz
Transmitter IF amp gain range		-10		20	dB
Output power step size			6		dB
# power steps			5		
Transmitter output power				10	dBm

Vdd = 5.0V, 25°C

Chip Status

- 2nd pass chip submitted to AMI for fabrication
- Expect parts from fab by 20 July, 2004

Application Demonstration

- VDL mode-3 data link
  - Pressing need to get better information to pilots
  - Better info improves flight safety
  - Weather is a significant cause of fatal accidents

Why a Data Link Demonstration?

Would you rather have this?

2004/04/06 17:20 KBJI 061720Z 061818 33012KT P6SM SKC FM0000 VRB06KT P6SM SCT250 FM0800 15007KT P6SM SCT120 TEMPO 1115 BKN080 FM1500 18007KT P6SM BKN080 PROB30 1518 -RA OVC030

Why a Data Link Demonstration?

Or, would you prefer this:

A picture just might be worth more than 1000 words...

Data Link Demonstration

- Data links can provide rich and varied information
- Bidirectional data links allow the pilot to request specific information not otherwise available

Demonstration radio is intended to prove a concept, leading to a product

Conclusion

- Radio-on-a-chip can tailored to meet specific requirements
  - Product life-cycle costs can be significantly reduced
  - High initial cost requires careful consideration in deciding to design your own chips
- High levels of integration are possible
  - results in potentially significant reductions in circuit board complexity